ISSN: 2096-3246
Volume 54, Issue 02, December, 2022

Special Issue

# LEAKAGE POWER MINIMIZATION USING GATING TECHNIQUE IN CMOS DESIGN CIRCUITS

**Dr.T.Joby Titus**
Dhanalakshmi Srinivasan College of Engineering, Coimbatore, Tamil Nadu, India

**R.Arun Prasath**
Dhanalakshmi Srinivasan College of Engineering, Coimbatore, Tamil Nadu, India
jobyece007@gmail.com

**Nitin Jain**
Babu Banarasi Das University, Lucknow (U.P.) India

**Abstract:** In our day-to-day life the application of the electronic device plays a major role. As the technology develops the size of the devices are being decreased. It leads to wide usage of the FPGA devices and power consumption limits its application. The most of the electronic devices are battery operated devices. So power consumption is very essential criteria. The power consumption is based on static power and dynamic power. Static power consumption mainly depends on leakage power. The lookup table based fine grain power gating technique and effective utilization of logic block is used to reduce the leakage power. This technique is utilized to reduce the leakage power consumption in FPGA controlled device based on the concept of low power design and effective utilization of logic blocks.

**Keywords:** Power consumption, Fine grain, coarse grain, Lookup Table

## 1. INTRODUCTION

The Most of the Electronics Engineering are exposed to Integrated Circuits (IC's) at a very basic level, involving SSI (small scale integration) circuits like logic gates or MSI (medium scale integration) circuits like multiplexers, parity encoders etc. The scaling of devices in micrometer and nanometer range should not affect the performance of the circuit and doesnot cost the power consumption. The innovation in VLSI technologies are used for design of many application like computer, digital camera, the cell-phones etc.

FPGA stands for Field Programmable Gate Array and it can be programmed and configured by the embedded system developer in the field once it is manufactured. Most of FPGA is not limited to any pre-defined hardware function and use pre-built logic blocks and programmable routing channels for implementing custom hardware functionality depending upon how embedded system developer configure these devices. The configuration of FPGA devices can be achieved using hardware description languages. The market of FPGAs is growing at an enormously high rate and popularity of FPGAs is growing day by day. FPGA provides design flexibility and can be programmed by the end-user. The logic functions with Application-Specific Integrated Circuit (ASIC) is possible using FPGA

The proposed work is focussed on reconfigurable circuits to minimize leakage current using Lookup table enabled gating techniques. The rest of the paper is organized in such a way that section 2 explains the background work on gating techniques and power consumption. Section 3 briefs the proposed work and section 4 shows the results. The proposed work is concluded in section 5.

## 2. BACKGROUND WORK

The power consumption in FPGA devices is categorized under static and dynamic activities. In CMOS logic, which includes SRAM-based FPGAs, leakage current is the only source of static power dissipation. There are two major sources of leakage current:

- Reverse biased PN-junction current
- Sub-threshold channel conduction.

Both these components have similar characteristics such as high dependency to temperature, process variation, and logic states of the circuit. In most of the researchers the leakage current is ignored and it is one of the demanding factor during transistor scaling. Scaling often comes with a reduction in power supply voltage (Vdd), and lower Vdd reduces the speed. To maintain or increase the speed we need to reduce the threshold voltage (Vth) of the transistor along with the scaling. The impact of static power exponentially increases with decrease in Vth. The importance of static power dissipation in future FPGAs and on the dynamic components of power dissipation are analyzed. According to our empirical results, the static power is between 5-20% of total power dissipation in Virtex-II, depending on the temperature, device, running frequency, and the design.

### 2.1 Dynamic Power Consumption

The signal transition of the circuit leads to dynamic power dissipation. A higher operating frequency leads to more frequent signal transition and results in increased power dissipation. The impact of charging and discharging of capacitance leads to increase in dynamic power consumption in active mode of CMOS circuits. This can be modeled as

$$P = \sum_i C_i V_i^2 f_i$$

where Ci, Vi, and fi represent the capacitance, voltage swing, and operating frequency of the circuit. The short circuit power in CMOS transistor occurs due to signal switching rate. According to our simulations, short-circuit current in FPGA interconnect is less than 10% of the total. This is consistent with the literature because interconnect short-circuit power dissipation is mostly caused by switching of inverters in the buffers. In CMOS circuits the short circuit power of CLB slice is of higher percentage of its total power consumption. We emulate short-circuit power with an additional capacitance.

**The power estimation is done with three parameters:**

- The effective capacitance as the sum of parasitic effects due to interconnection wires and transistors.
- The resource utilization of CMOS configurable circuits, the majority of the resources remains unused and does not contribute to dynamic power. Since the resource utilization varies with

design.

- The third factor in determining power dissipation is the switching activity, which is defined as the number of signal transitions in a clock period.
  For example, a clock signal has as switching activity of two. A statistical representation is required to determine the switching activity as it depends not only on the type of design, but also the input.

### 2.2. Leakage power in Active Mode

In modern commercial CMOS processor, the contribution of leakage power dissipation in buffers and multiplexers is typically smaller when the output and input of these structures is logic 1 versus logic 0.

The leakage power optimization approach is analyzed by choosing the polarity for each signal that spend the majority of their time in the logic 1 state (the logic state associated with low leakage power). The static probability of digital signal is the fraction of time a signal spends in the logic 1 state. A signal with static probability greater than 0.5 spends more than 50% of its time at logic 1. The static probability of signal alters the signal polarity. Unlike in ASICs, signal polarity inversion in FPGAs can be achieved without any area or delay penalty, by leveraging a unique property of the basic FPGA logic element.

### 2.3. Leakage power in Sleep Mode

In sleep mode, the sleep transistor can be used to reduce the subthreshold leakage in peripheral circuits. The various sleep mode is used for non volatile FPGAs. Sleep Modes and other low power modes are involving powering down the device and turning it back on when needed. It is an on/off switch approach. that the sleep transistor is connected between actual ground and circuit ground. The sleep transistor circuit is shown in the figure 1.

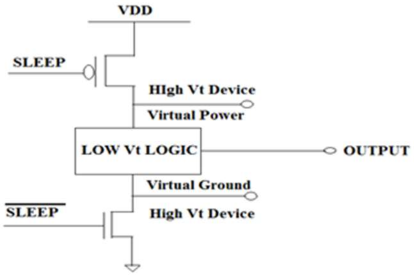
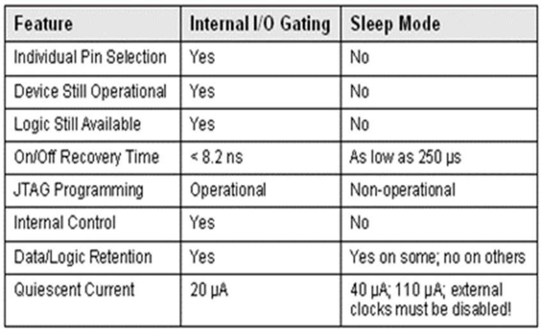


Fig1: Sleep Transistor with variable voltage rate



| Feature | Internal I/O Gating | Sleep Mode |
|---|---|---|
| Individual Pin Selection | Yes | No |
| Device Still Operational | Yes | No |
| Logic Still Available | Yes | No |
| On/Off Recovery Time | < 8.2 ns | As low as 250 µs |
| JTAG Programming | Operational | Non-operational |
| Internal Control | Yes | No |
| Data/Logic Retention | Yes | Yes on some; no on others |
| Quiescent Current | 20 µA | 40 µA; 110 µA; external clocks must be disabled! |

Table 1: Sleep Transistor features

## 3. PROPOSED METHOD

FPGA are widely used to implement special-purpose processors. FPGAs are cost-effective for small-lot production because functions and interconnections of logic resources can be directly programmed by the users. These overheads increase packaging costs and limit integrations of FPGAs into portable devices .As the transistor sizes and threshold voltages decrease, the standby power due to leakage current becomes comparable to dynamic power. Especially, in FPGAs, the standby power is a serious problem because it has an large number of transistors to achieve its programmability. The power consumption of power gating circuitry is consumed by the sleep controller, the sleep signal distribution network and the sleep transistors. In power gating technique the standby power overhead plays the major contributor in overall power consumption. Power gating techniques are classified into two types:

1).Coarse-grain power gating.
2).Fine-grain power gating

In coarse-grain power gating, a large number of lookup tables share a single sleep controller so the area and power overheads of the sleep controller are relatively small. In coarse grained gating technique within the CLB block if any LUT is in active state then the entire LUT block is made to active state. Another parameter in coarse-grain power gating approach is the dynamic power and area overhead due to the distribution of sleep transistor.

In fine-grain grain approach, individual sleep transistor with controller plays a major role and the sleep transistor disables the LUTs. This results in much lower standby power compared to coarse-grain power gating. In fine-grain power gating, each LUT has its sleep controller, the number of sleep controllers is much larger than that of coarse-grain power gating. So we use fine grain gating techniques.

### 3.1. Look up Table:

Look up Tables (LUT) is a bunch of single bit memory cells storing individual bit values in each of the cells. To implement a 2 input AND-gate using LUT. It stores 0, 0, 0, and 1 in addresses 00, 01, 10 and 11 respectively. Now you inputs become your address lines. So, when inputs are 0 and 0 the output of LUT is 0.

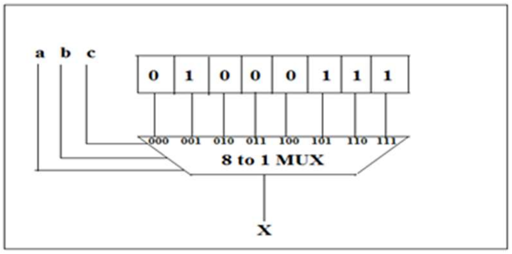


Fig 2: Representation of 3 input LUT

Fig 3: LUT operation

The logic cell contains switching blocks, logic block and pass-switch block. The switching blocks means the most of the FPGA area is due to routing

- Fixed metal tracks arranged in horizontal and vertical channels.
- Connected to each other using switch blocks.

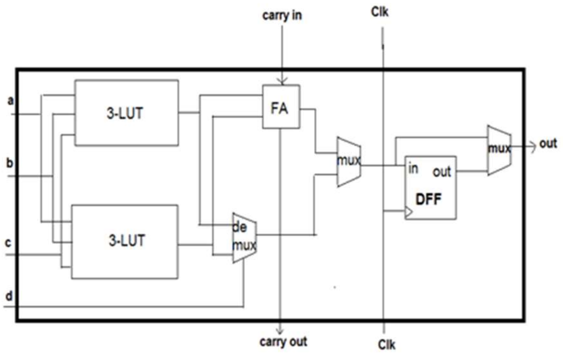


Fig 3: 3 Input LUT

### 3.2 Sleep Transistor:

The sleep transistor is used to reduce the leakage power in FPGA circuits. It is an effective way to reduce the leakage of a transistor is thus increasing its source voltage.

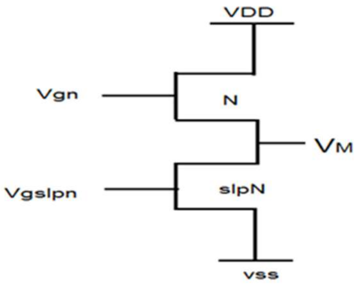


Fig 4: Variable rate Sleep Transistor

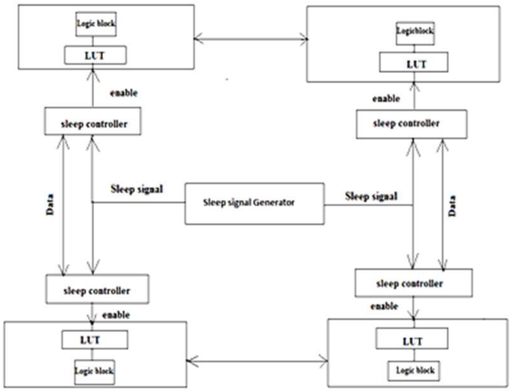


Fig 5: Block Diagram of Proposed Method

Sleep transistor designed with transistor N and splN to reduce the sub threshold leakage current when both transistors are OFF. The leakage reduction is related to the virtual ground voltage(VM) during the sleep mode which is turn is determined by the size of sleep transistor and bias voltage(Vgslpn), while increasing the circuit transition wakeup period because up transistor N requires puling down the voltage VM to ground. Also the stacking sleep transistor would make all high voltage nodes to discharge during the standby mode due to large leakage current of the circuit

## 4. RESULTS AND DISCUSSION

The proposed approach is analysed with Mwind simulation tool to estimate the leakage power based on the lookup table activity. The leakage power is compared in both proposed approach and existing gating methods

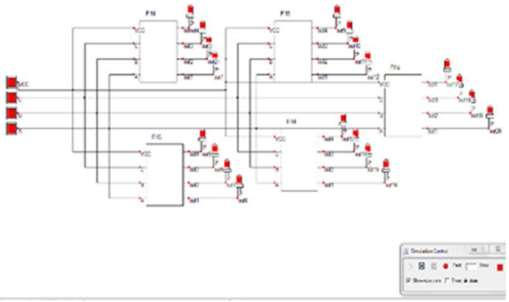


Fig 6: Logic diagram of existing method with no LUT

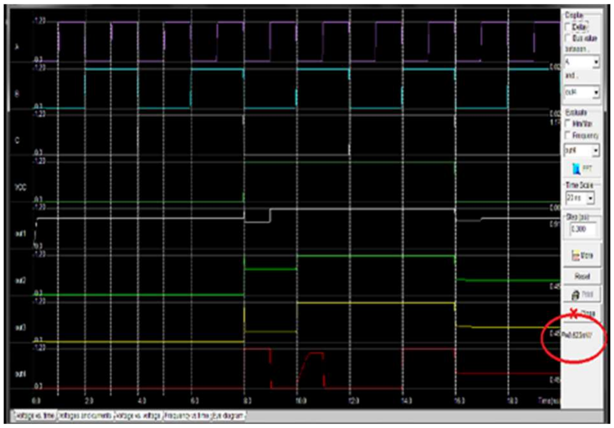


Fig 7: Power and logic activity of existing method with no LUT

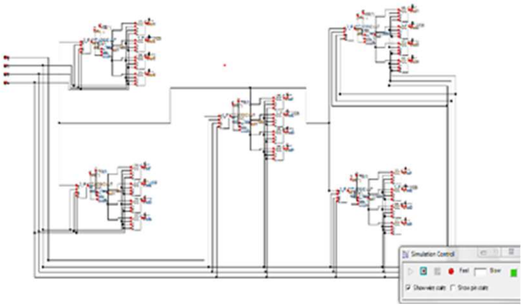


Fig 8: Proposed method logic block

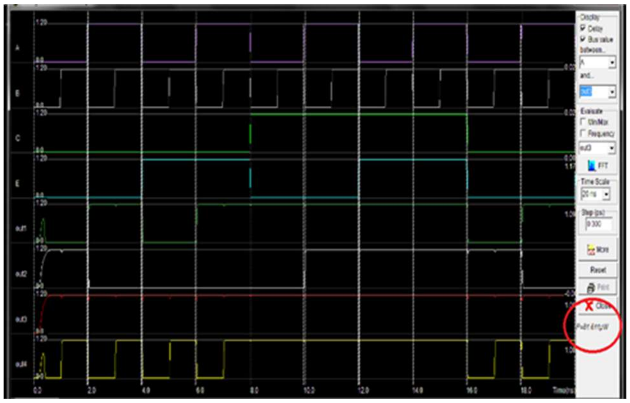


Fig 9: Power and logic activity of proposed gating techniques

**Table 2: Power consumption comparison**

| Existing Method Without LUT | Proposed Method |
|---|---|
| Power=0.632mW | Power=0.0816mW |

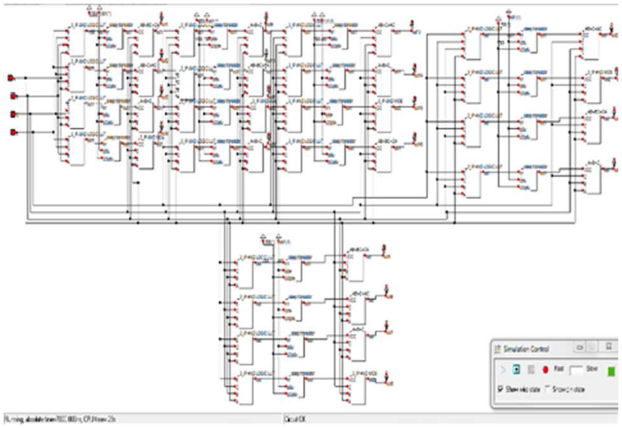


Fig 10: Logic diagram of existing method with separate LUTs

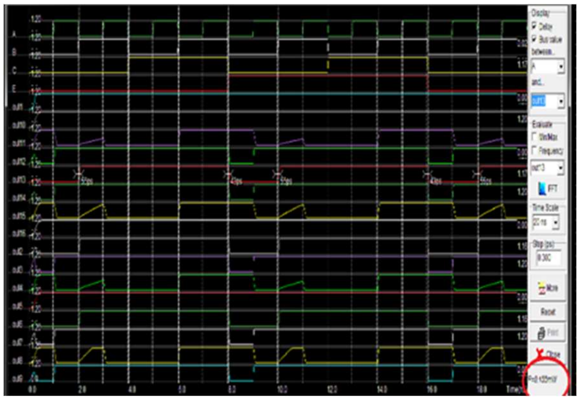


Fig 11: Simulation results of existing method with separate LUTs

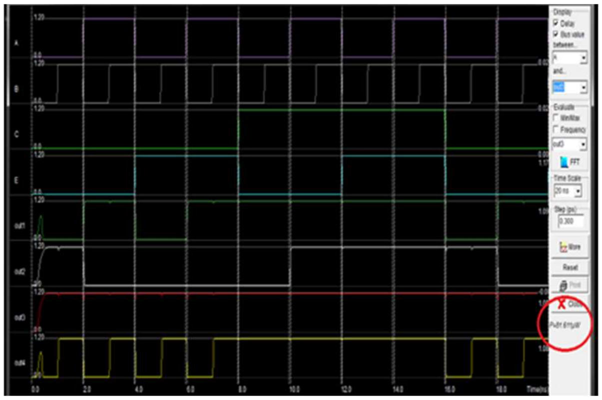


Fig 11: Simulation results of proposed method using Gated LUTs

**Table 3: Power consumption comparison**

| Existing Method with separate LUT | Proposed Approach |
|---|---|
| Power=0.155mW | Power=0.0816mW |

## 5. CONCLUSION:

The proposed fine grain power gating technique analyses the leakage power based on the logic activity of LUT. The logic activity is detected by comparing the phases of the input and the output data. The standby state is used to wake up the logic block before the data arrives and power OFF the logic block only when the data does not come in sleep mode. The wakeup timing of sleep transistor is controlled to limit unnecessary switching of transistor. Hence, the fine grain gating technique is also suitable for dynamically reconfigurable processors which work toward self-adaptation for ambient intelligence. The variation in data paths limits to determine the control parameters for each logic block using offline analysis.

## References

[1]Shota Ishihara, Student Member, IEEE, Masanori Hariyama, Member, IEEE, andMichitaka Kameyama, Fellow, IEEE “A Low-Power FPGA Based on Autonomous Fine-Grain Power Gating”

IEEE transactions on very large scale integration systems, vol. 19, no. 8, august2011

[2]Andy Gean Ye,( 2010), "Using the Minimum Set of Input Combinations to Minimize the Area of Local Routing Networks in Logic Clusters Containing Logically Equivalent I/Os in FPGAs", IEEE TRANSACTIONS ON VLSI SYSTEMS, VOL. 18, NO. 1.

[3]Mingjie Lin and Abbas El Gamal,( 2009), "A Low-Power Field-Programmable Gate Array Routing Fabric" , IEEE VLSI SYSTEMS, VOL. 17, NO. 10.

[4]M. Hariyama, S. Ishihara, and M. Kameyama, (2008 ),"Evaluation of a field programmable VLSI based on an asynchronous bit-serial architecture," IEICE Trans .Electron, vol. E91-C, no. 9, pp.1419–1426.

[5]Y. Ahmed, A. Mohab, and E. Mohamed, (2008 ),"A comparative study between static and dynamic sleep signal generation techniques leakage tolerant designs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 9, pp. 1114–1126.

[6]T. Tuan, S. Kao, A. Rahman, S. Das, andS. Trimberger,( 2006), "A 90 nm low-power FPGA for battery-powered applications," in Proc.FPGA, pp. 22–24.

[7]F. Li, Y. Lin, L. He, and J. Cong, "Low-power FPGA using pre-defined dual-Vdd/dual-Vt fabrics," in Proc. 2004 ACM/SIGDA 12th Int. Symp. Field-Programmable Gate Arrays, 2004, pp. 42–50.

[8]J. H. Anderson, F. N. Najm, and T. Tuan, "Active leakage power optimization for FPGAs," in Proc. ACM Intl. Symp. Field-Programmable Gate Arrays, Februray2004.

[9]N. Gupta, "Thermal analysis of energy efficient clock gated arithmetic logic unit on FPGA," 2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), Kanyakumari, 2014, pp.990-993.

[10]S. Chtourou, M. Abid, Z. Marrakchi and H. Mehrez, "Power consumption analysis for mesh based FPGA," 2014 9th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), Santorini, 2014, pp. 1-5.