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# POWER-OPTIMIZED 4-BIT FULL ADDER USING GDI AND ADIABATIC LOGIC IN FINFET TECHNOLOGY

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**Abstract -** The increasing demand for energy-efficient and high-performance digital systems has made the design of low-power arithmetic circuits a critical area of research. Full adders, being core components of arithmetic logic units (ALUs), play a vital role in determining the overall efficiency of digital architectures. This paper presents a novel Low-Power Hybrid 4-bit Full Adder design utilizing 14nm FinFET technology to address the challenges of power consumption and speed in modern computing applications. The proposed architecture combines Gate Diffusion Input (GDI) logic with Energy-Efficient Diode-Connected DC Biased Positive Feedback Adiabatic Logic (EE-DC-DB PFAL), leveraging both logic minimization and adiabatic switching to enhance power performance. FinFET devices are employed to exploit their superior electrostatic control and reduced leakage characteristics at the nanoscale. Comprehensive simulations conducted using industry-standard tools demonstrate significant improvements in power dissipation, delay, and energy efficiency compared to traditional CMOS-based full adder designs. The results validate the effectiveness of the proposed hybrid approach, making it a promising candidate for integration into low-power digital processing units and future ultra-scaled VLSI systems.

**Keywords:** Low-power design, 4-bit full adder, FinFET, GDI logic, EE-DC-DB PFAL, adiabatic logic, hybrid VLSI circuits

## 1. Introduction

The growing demand for low-power, high-performance digital systems in portable and wearable devices has intensified the need for energy-efficient circuit design. The full adder, being a core element of arithmetic and logic units, significantly impacts power and delay in larger systems, making its optimization critical.

Conventional CMOS scaling below 20 nm faces challenges such as increased leakage and degraded electrostatic control. FinFET technology addresses these issues through multi-gate architecture, offering improved control, lower leakage, and better scalability for nanoscale circuits.

In parallel, logic-level innovations like Gate Diffusion Input (GDI) reduce transistor count and dynamic power, while adiabatic logic minimizes switching losses by enabling energy recovery. This paper proposes a hybrid 4-bit full adder architecture combining GDI logic and a novel EE-DC-DB PFAL (Diode-Connected, DC-Biased Positive Feedback Adiabatic Logic) style for sum and carry generation, implemented using 14 nm FinFET technology.

Key contributions include:

- A low-power EE-DC-DB PFAL logic family using diode-connected FinFETs and DC bias for leakage control and energy recovery.
- Design of core gates (XOR/XNOR) and a 1-bit hybrid full adder combining GDI and adiabatic logic.
- Implementation of a 4-bit ripple-carry adder evaluated at 14nm technology node and power-clock frequencies (100–500 MHz).
- Comparative benchmarking showing reduced power and PDP against existing full adder designs.

The paper is organized as follows: Section 2 covers background on FinFETs and Energy-Efficient Design techniques. Section 3 details the design methodology and architectural overview of the proposed circuit. Section 4 outlines the simulation setup and analysis. Section 5 presents performance comparison and benchmarking. Section 6 concludes the work.

## 2. Overview of FinFET and Energy-Efficient Design Approaches

### 2.1 FinFET Technology

As transistor dimensions shrink below 20nm, planar CMOS devices face challenges such as short-channel effects (SCEs), leakage currents, and poor gate control. FinFETs, a three-dimensional transistor with a fin-shaped channel surrounded by multiple gates, address these issues. The multi-gate design improves electrostatic control, reducing off-state leakage and enhancing scalability and drive current. FinFETs are ideal for high-density, low-power applications in advanced VLSI systems, with successful implementation down to 7nm. This study uses a 14nm FinFET node optimized for low-power logic with reduced leakage and high performance[1].

### 2.2 Background on Advanced Low-Power Design Techniques

The limitations of conventional CMOS logic in terms of dynamic power consumption have led to the exploration of alternative logic design styles aimed at improving energy efficiency. Two such prominent techniques are adiabatic switching circuits and Gate Diffusion Input (GDI) logic. These approaches reduce energy consumption either by recycling energy during logic transitions or by minimizing transistor usage and internal capacitance.

#### 2.2.1 Adiabatic Switching and EE-DC-DB PFAL

Adiabatic logic utilizes energy-recovering switching principles, where capacitors charge and discharge slowly through controlled power clocks, allowing partial recovery of stored energy. Among several adiabatic families, Positive Feedback Adiabatic Logic (PFAL) is widely used for its robustness and recoverability. The Energy-Efficient Diode-Connected DC-Biased PFAL (EE-DC-DB PFAL) has been proposed in this paper which further enhances energy efficiency by using diode-connected FinFETs and static DC biasing to minimize leakage. This technique is highly effective at nanometre-scale nodes, where leakage and energy loss are predominant[2], [3].

#### 2.2.2 Modified Gate Diffusion Input (MGDI) Logic

The MGDI (Modified Gate Diffusion Input) technique is an evolution of the standard GDI logic, designed to address the limitations of signal degradation and limited logic functionality in deep submicron technologies. In MGDI, improved biasing techniques and alternative transistor configurations are used to maintain full logic swing and reduce threshold voltage drop issues commonly seen in basic GDI designs. This technique allows complex logic functions to be realized

using fewer transistors compared to CMOS, leading to reductions in area, power dissipation, and propagation delay. MGDI is particularly effective in arithmetic circuits like full adders, multiplexers, and comparators where low power and high-speed operation are required in limited silicon area.

By combining these two complementary approaches—MGDI for compactness and switching efficiency, and a novel adiabatic logic EE-DC-DB PFAL for energy recovery—this work presents a hybrid low-power 4-bit full adder architecture implemented in FinFET technology. This hybrid design is evaluated for its performance in terms of power dissipation, delay, and energy efficiency, offering a viable solution for future energy-constrained computing environments[4].

## 3. Design Methodology

This section presents the systematic design approach for the proposed low-power hybrid 4-bit full adder. The methodology integrates a novel energy-efficient adiabatic logic style with a Modified Gate Diffusion Input (MDI) strategy, all implemented using 14nm FinFET technology to achieve superior power-delay performance. The design consists of four cascaded 1-bit full adders, each comprising two functional stages: adiabatic XOR/XNOR generation and MDI-based carry and sum logic.

### 3.1 Architectural Overview of the Hybrid 4-bit Adder

The proposed 4-bit adder follows a ripple carry architecture, constructed by chaining four identical 1-bit hybrid full adders as shown in Fig .1. The 1-bit full adder is a fundamental arithmetic circuit

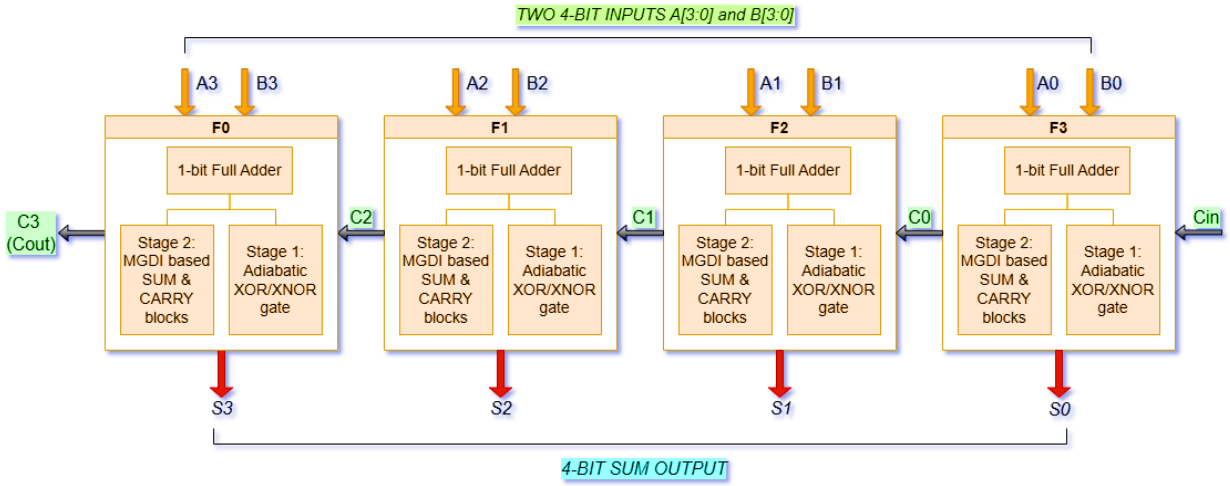


**Fig. 1 Block Diagram of the Proposed 4-bit Hybrid Full Adder Architecture**

responsible for adding three binary inputs: A (First operand), B (Second operand) and Cin (Carry-in from the previous stage). It generates two outputs: SUM (Sum of the inputs) and Cout (Carry-out to the next stage)[5].

Each 1-bit full adder is divided into two stages as illustrated in Fig. 1:

Stage 1: XOR and XNOR functions are realized using the proposed adiabatic EE-DC-DB PFAL logic.

Stage 2: The sum and carry logic are implemented using Modified GDI (MGDI) circuits for compactness and reduced dynamic power

By integrating adiabatic logic with a Modified Gate Diffusion Input (MGDI)-based design, the proposed full adder achieves superior energy efficiency, reduced power consumption, and enhanced overall performance, making it ideally suited for contemporary low-power VLSI applications. This dual-stage hybrid logic structure ensures a balanced trade-off between low-energy operation, functional scalability, and transistor-level optimization across all bit positions at the nanometre scale. The hybrid methodology effectively exploits the strengths of both techniques, enabling high-speed operation with minimal energy loss and promoting efficient energy reuse throughout the computation process.

### 3.2 Proposed EE-DC-DB PFAL Logic for Adiabatic XOR/XNOR

A key innovation of this work is the introduction of a novel adiabatic logic style—Energy-Efficient Diode-Connected DC-Biased Positive Feedback Adiabatic Logic (EE-DC-DB PFAL)—designed to implement low-power XOR and XNOR functions. This architecture builds upon conventional

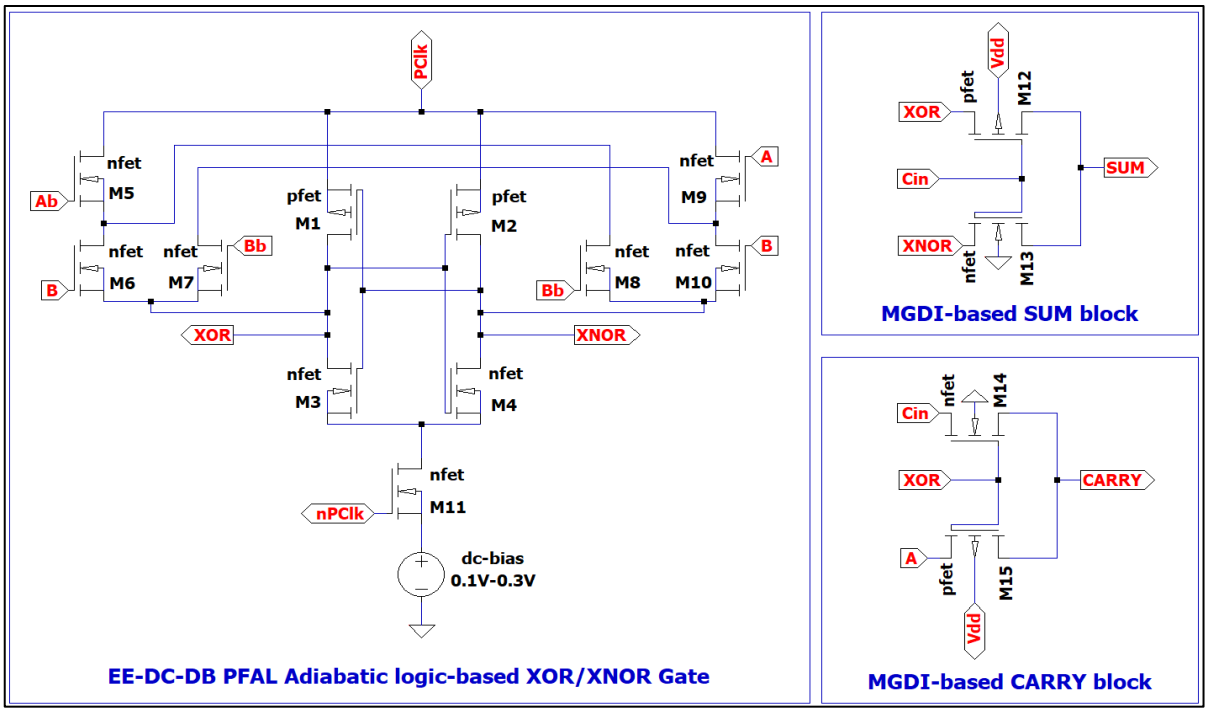


**Fig. 2 Schematic of proposed Hybrid 1-bit Full adder**

Positive Feedback Adiabatic Logic (PFAL), incorporating key enhancements to boost energy efficiency, signal integrity, and scalability at technology nodes below 20 nm[6].

The proposed EE-DC-DB PFAL integrates several key innovations to enhance energy efficiency and reliability in nm-scale circuits. Diode-connected FinFETs are placed at the output stage to suppress reverse current flow and minimize leakage, ensuring robust signal restoration even at reduced supply voltages. A DC biasing scheme is applied at intermediate nodes to stabilize threshold voltages and maintain full-swing outputs across process-voltage-temperature (PVT) variations. The logic core features a positive feedback structure formed by cross-coupled inverters, which improves noise

margins and supports non-volatile logic retention during the recovery phase. Additionally, the circuit employs adiabatic switching via a four-phase trapezoidal power-clock waveform, allowing gradual charging and discharging of internal nodes to enable partial energy recovery and significantly reduce dynamic power dissipation[7].

This circuit in Fig. 2 is a dual-function adiabatic XOR/XNOR gate using FinFET-based EE-DC-DB PFAL (Energy Efficient Diode Connected DC Biased Positive Feedback Adiabatic Logic) design. It uses both PFETs and NFETs, driven by complementary power clocks (PCIk and nPCIk), along with a DC-bias voltage in the range of 0.1V–0.3V to enhance energy efficiency. M1 (PFET) and M3 (NFET) form the left latch. M2 (PFET) and M4 (NFET) form the right latch [8]. These transistors create a cross-coupled latch structure, central to PFAL logic, which facilitates energy recovery by maintaining the output logic level and allowing charge to flow back to the power clock (PClk) during the discharge phase, thereby improving energy efficiency. PCIk is connected to sources of M1 and M2 (PFETs). It's the main power-clock (ramping up/down instead of being constant). A nPCIk is connected to the source of M11 (NFET), acts as the inverse of PCIk, used to discharge the circuit or assist in recovery. The transistors M5–M10 implement the XOR and XNOR logic using complementary inputs (A, Ab, B, Bb). Specifically, M9 and M10 contribute to the correct evaluation of the XNOR output based on the input combinations. Meanwhile, transistor M11, controlled by nPClk, aids in discharging excess charge from the internal nodes to ground, assisted by the applied DC bias (0.1V–0.3V) to reduce energy loss. A positive DC voltage source connected between the diode and the ground utilize the benefits of level-shifting technique and lowers the gate-to-source voltage at the output transistor, thereby reducing both gate and leakage currents, which results in lower power dissipation compared to conventional PFAL logic. Additionally, the adiabatic power clocking scheme plays a crucial role in enabling energy-efficient switching. Combined with the circuit's transistor configuration, it ensures correct logic functionality and optimal performance in the adiabatic computing domain.

This logic is employed in the first stage of the hybrid full adder to compute XOR (A, B) and XNOR (A, B), which serve as essential intermediate signals for subsequent sum and carry generation. By operating on energy-recycling principles and leveraging FinFET advantages, EE-DC-DB PFAL provides considerable power savings compared to conventional CMOS and even baseline adiabatic designs. The proposed EE DC-DB PFAL achieves power dissipation as low as 771.2pW at 0.1 DC - bias for XOR/XNOR gates using 14nm FinFET technology. In contrast, other adiabatic families exhibit dissipation in the nanowatt range, ranging from 5.517nW to 14.8nW. The substantial improvement in energy efficiency is attributed to the adoption of finfet technology, which minimizes leakage and enhances performance. Simulation results highlight the significant reductions in both average power and energy-per-operation metrics in the proposed EE DC-DB PFAL making it a highly efficient solution for ultra-low-power applications, particularly in modern integrated circuits demanding reduced energy consumption[9].

### 3.3 MGDI-Based Sum and Carry Logic Blocks

The Gate Diffusion Input (GDI) technique minimizes power, delay, and area while preserving low design complexity. A GDI cell uses three inputs: G (common gate for PMOS/NMOS), P (PMOS source/drain), and N (NMOS source/drain). Connecting the bulk terminals to P and N reduces

leakage currents, making it more efficient than standard CMOS.

The Modified GDI (MGDI) technique, an advanced variant of GDI further extends the capabilities of traditional GDI by fixing PMOS and NMOS bulk terminals to Vdd and Gnd, respectively. This adjustment not only reduces power losses but also resolves the degraded output swing typically encountered in standard GDI circuits, thereby improving signal integrity and enabling more reliable low-power VLSI design.

In the proposed hybrid 1-bit full adder architecture from Fig. 2, each 1-bit full adder employs Modified Gate Diffusion Input (MGDI) logic in stage 2 for computing SUM and Carry outputs efficiently, offering significant improvements in energy efficiency, area reduction, and logic simplicity.

The MGDI-based SUM block behaves like a 2:1 multiplexer, using transistors M12 and M13. The carry-in (Cin) signal acts as the select line, choosing between XOR and XNOR outputs:

- Cin = 0 → SUM = XOR (A, B)
- Cin = 1 → SUM = XNOR (A, B)

Thus, the SUM output is expressed as:

$$\text{Sum} = A \oplus B \oplus Cin \tag{1}$$

$$\text{Sum} = \overline{Cin}(A \oplus B) + Cin\ (\overline{A \oplus B}) \tag{2}$$

The Carry generation block, uses M14 (nFET) and M15 (pFET) in a parallel pull-up/pull-down MGDI structure. The output Carry is derived using simplified XOR-based logic:

$$\text{Cout} = (A \oplus B)Cin + (A \oplus B)A \tag{3}$$

Here:

- (A ⊕ B) Cin represents carry propagation, and determines how the input carry Cin propagates based on A⊕B.
- (A ⊕ B) A represents carry generation and ensures that a carry is generated when both A and B contribute to a high output.

M14 connects Cin to the carry output. When both A ⊕ B = 1 and Cin = 1, M14 activates and pulls the output LOW.

M15, controlled by A and A ⊕ B, drives the output HIGH when A = 1 and A ⊕ B = 1, enabling efficient carry generation.

By cascading these MGDI-based 1-bit blocks, the full 4-bit adder benefits from reduced power, area, and leakage, while maintaining reliable logic evaluation under adiabatic operation.

**4. Simulation Analysis**

To validate the practical feasibility and efficiency of this proposed hybrid 4-bit full adder in modern VLSI design, simulations were conducted using 14-nm finfet technology, which is known for its superior scalability, reduced leakage, and enhanced switching characteristics. The results of these simulations provide critical insights into the power, delay, and energy efficiency metrics of the proposed circuit.

The proposed 4-bit full adder, designed using cascaded 1-bit full adder logic blocks, was implemented and simulated using the Cadence Virtuoso design environment. The simulations were

**Table 1: 14−NM FinFET Device Parameters**

| *Technology node* | 14nm |
|---|---|
| *Gate length (Lg)* | 18n |
| *Fin height (Hfin)* | 23n |
| *Fin Width (Wfin)* | 10n |
| *Oxide thickness (tox)* | 1.3n |
| $V_{DD}$ | 0.8V |

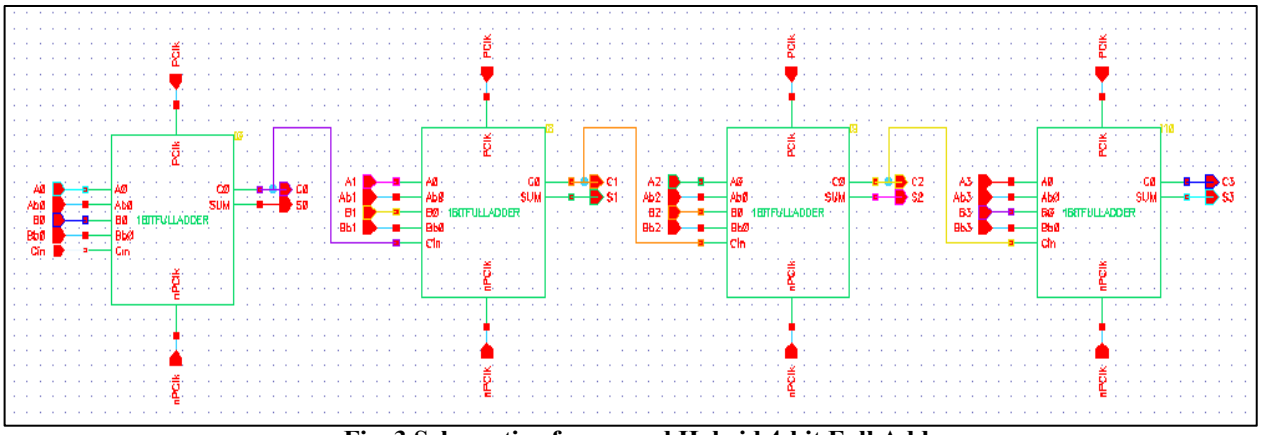


**Fig. 3 Schematic of proposed Hybrid 4-bit Full Adder**

**Table 2: Design Parameters**

| *Parameters to be measured* | Power (Watt), Delay (sec) & PDP |
|---|---|
| *Technology node* | 14nm FinFET |
| *PMOS $ NMOS width* | 56nm |
| *PMOS $ NMOS length* | 18nm |
| *Input Voltage* | 0.8V |
| *4-bit Input frequency (A[3:0, B[3:0])* | (50 Hz, 25 Hz) |
| *Rise time of PClk* | 1ns |
| *Fall time of PClk* | 1ns |
| *PClk Voltage (Vdd)* | 0.8V |
| *PClk Frequency* | 100MHz,200MHz,500MHz |
| *Transition time* | 100ns |
| *DC values for proposed logic* | 0.1-0.3V |

carried out using a 14nm FinFET Process Design Kit (PDK) taken from the website of University of Minnesota, USA, enabling accurate device-level modelling under scaled technology conditions. Table 1 outlines the device parameters of 14-nm FinFET technology used in the simulation of proposed EE DC-DB PFAL based XOR/XNOR logic gate and further hybrid 4-bit full adder circuit design.

The 1-bit full adders are connected in a ripple-carry configuration to create the 4-bit adder, operating

with a sinusoidal power-clock (PClk) of 0.8V peak amplitude, evaluated at frequencies of 100 MHz, 200 MHz, and 500 MHz. Table 2 summarizes the design parameters used for simulations in Cadence Virtuoso with the Spectre simulator, utilizing 14-nm FinFETs under zero load capacitance. A complementary power-clock (nPClk) is phase-shifted by 180° to enable bidirectional energy transfer during adiabatic switching. The PClk rise and fall times are set to 1 ns, with a transition interval of 100 ns to ensure smooth charge recovery and minimize dynamic losses[10].

The power clocking scheme, detailed in Table 3, specifies voltage levels, frequencies, and transition times to ensure efficient energy recovery, reduced energy dissipation, and synchronization across modules. Additionally, a positive DC bias (0.1V to 0.3V) is applied to diode-connected transistors

**Table 3: Adiabatic Power Clocking scheme for the design of 1-bit Full Adder**

| *Components* | *Vdc (V)* | *Tr (ns)* | *Tf (ns)* | *Freq (MHz)* | *Delay (ps)* |
|---|---|---|---|---|---|
| *PClk* | 0.8 | 1ns | 1ns | 100 | 50p |
| *nPClk* | 0.8 | 1ns | 1ns | 50 | 50p |
| *I/P A* | 0.8 | 0 | 0 | 12.5 - 100 | 0 |
| *I/P Ab* | 0.8 | 10p | 10p | 12.5 - 100 | 0 |
| *I/P B* | 0.8 | 20p | 20p | 12.5 - 100 | 0 |
| *I/P Bb* | 0.8 | 10p | 10p | 12.5 - 100 | 0 |
| *I/P Cin* | 0.8 | 10p | 10p | 6.25 | 0 |

for improved logic threshold control and enhanced energy efficiency.

To evaluate the functionality and energy efficiency of the proposed 4-bit adiabatic full adder, all eight input combinations for the operand bits A [3:0] and B [3:0], along with the carry-in (Cin), are applied sequentially. Input signals A and B are binary vectors, incremented from 0000 to 1111 whereas Carry-in (Cin) is toggled between 0 and 1 to evaluate its effect on sum and carry propagation. All input transitions are synchronized with the adiabatic power-clock (PClk).

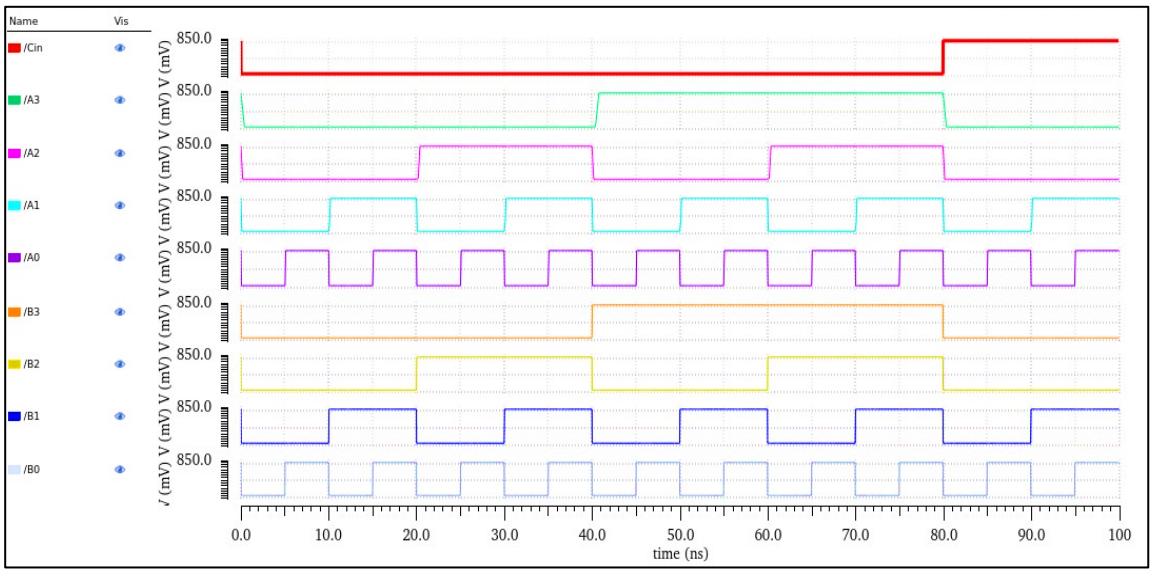


**Fig. 4: Input waveforms with binary counting A[3:0], B[3:0], and Cin to proposed hybrid 4-bit full adder with transition at 80 ns**

For reliable simulation of a 4-bit full adder using 14nm FinFETs, input signal frequencies should be chosen to allow sufficient time for logic evaluation and to avoid glitches. A practical approach is to generate input patterns using binary counter behaviour for A[3:0] and B[3:0], where the least significant bits A0 and B0 toggle at 50 MHz, and each successive bit toggles at half the frequency (A1/B1 at 25 MHz, A2/B2 at 12.5 MHz, A3/B3 at 6.25 MHz). The carry-in (Cin) should toggle much slower, ideally around 1–5 MHz, to simulate both carry propagation and ripple effects properly. These frequencies ensure that transitions are well within the circuit's response time and enable accurate observation of sum and carry behaviour during simulation. This is reflected in the provided input waveform graph in Fig. 4, where A and B inputs follow a binary counting pattern, and Cin changes state only once around 80 ns, allowing clear analysis of how the full adder responds to different input combinations and the effect of carry-in.

The sum and carry outputs in the second graph (Fig.5) showing the output response, align with the 4-bit full adder truth table, accurately reflecting binary addition and carry propagation for each input combination of A, B, and Cin. For instance, when A = 0101, B = 0011, and Cin = 0, the sum output is correctly shown as 1000. As inputs increment and Cin toggles later in the simulation, the output

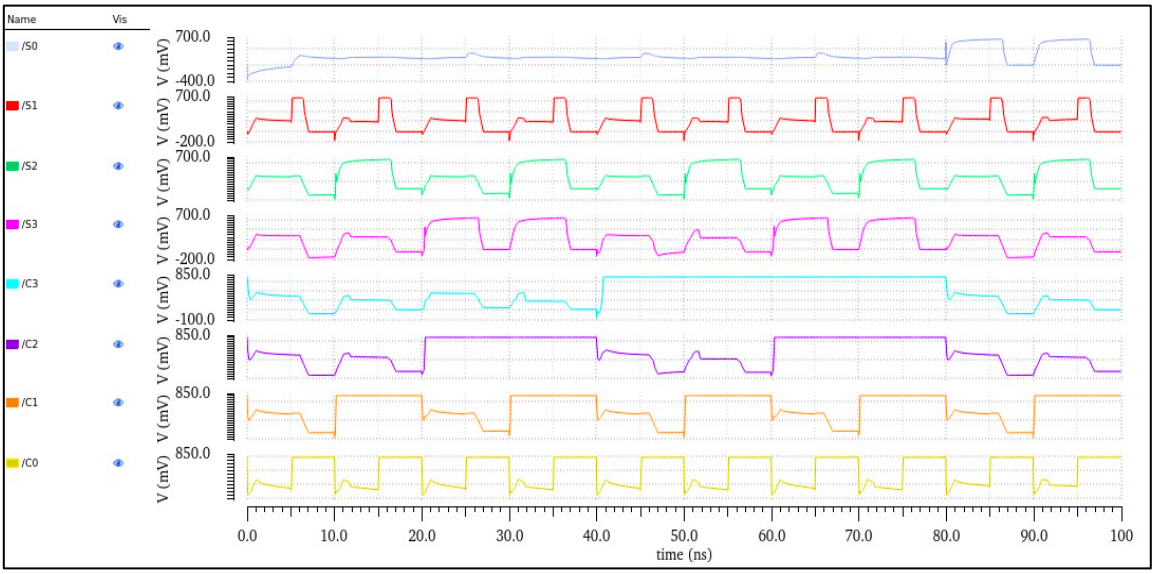


**Fig.5 Output response of proposed hybrid 4-bit full adder**

transitions continue to match expected results, confirming the functional correctness of the adder design.

Key performance metrics, including average power dissipation, propagation delay, and the power–delay product (PDP), are extracted to quantitatively assess the energy efficiency and timing behaviour of the proposed design. These key metrics indicate the overall performance of the proposed 4-bit full adder. This simulation setup ensures comprehensive testing across all possible input transitions, enabling accurate measurement of power dissipation, delay, and logic correctness under integration of adiabatic switching and Gate Diffusion Input (GDI) technique. The simulation results indicate a substantial reduction in power consumption while maintaining low propagation delay compared to conventional CMOS and FinFET-based adders.

**4. Performance Comparison and Benchmarking of Proposed Hybrid 4-bit Full Adder**

The Proposed Hybrid 4-bit Full Adder is evaluated against several benchmarked designs, as summarized in the Table 4. The Table 4 compares average power, critical path delay, and power-

**Table 4: Performance Comparison of the Proposed Hybrid 4-bit Full Adder with Benchmark Designs**

| 4-bit Full Adder design | Average Power (µW) | Critical path Delay (s) | PDP (fJ) | Reference |
|---|---|---|---|---|
| Adiabatic CSA [11] | 34.37 | 432.68 p | 14.8 | Sanjay Singh, 2015 |
| Hybrid Full Adder [12] | 1.65 | 325.8 p | 0.54 | M. Hasan, 2019 |
| Hybrid CLA Adder [13] | 38.82 | 0.135 n | 5.27 | Hossain & Arifin, 2021 |
| CMOS-based CLA [14] | 0.79 | 2.01 n | 1.589 | Suresh & Haasini, 2023 |
| GDI-based CLA [14] | 0.38 | 1.21 n | 0.459 | Suresh & Haasini, 2023 |
| FS-GDI Full Swing Adder [15] | 0.009 | 11 n | 0.099 | Zainudin et al., 2025 |
| Proposed Hybrid FA | 0.01165 | 0.98 n | 0.01142 | This work |

delay product (PDP) across different adder designs.

Average Power:

The Proposed Hybrid FA consumes 11.65 nW, which is much lower than designs like CMOS-based CLA (0.79 µW) and Adiabatic CSA (34.37 µW), indicating its superior energy efficiency.

Critical Path Delay:

The Proposed Hybrid FA has a critical path delay of 0.98 ns in the worst-case scenario, which is relatively high compared to some designs like the CMOS-based CLA (2.01 ns) but still faster than the FS-GDI Full Swing Adder (11 ns). The carry propagation delay from Cin to Cout is 214.9 ps, which is quite fast. However, the sum delay is more critical, as it involves additional adiabatic logic gates and specific circuit design elements that contribute to the higher delay of 0.98 ns.

PDP (Power-Delay Product):

The Proposed Hybrid FA has a PDP of 0.01142 fJ, the lowest among the designs, significantly outperforming the CMOS-based CLA (5.27 fJ) and Adiabatic CSA (14.8 fJ).

**Benchmarking Summary:**

The table demonstrates that the Proposed Hybrid FA strikes an excellent balance between low power and fast performance. Although the sum delay is higher due to the adiabatic logic design, the PDP remains the lowest, making it ideal for energy-efficient applications. The carry propagation delay (214.9 ps) is minimal, and the overall design is well-suited for low-power, high-performance systems.

## 5. Impact of Power Clock Frequency on Power Consumption

This section examines how changes in the frequency of the power clock influence the power consumption of the proposed hybrid 4-bit full adder design as shown in Table 5. The analysis highlights the relationship between power clock frequency and energy efficiency.

**Table 5: impact of increasing power clock frequency on power consumption**

| Power Clock Frequency (MHz) | Power Consumption (nW) |
|---:|---:|
| 100 MHz | 11.65 nW |
| 200 MHz | 14.57 nW |
| 500 MHz | 16.36 nW |

## 6. Conclusion

This study proposes a hybrid 4-bit full adder design integrating Modified GDI and EE-DC-DB PFAL techniques in 14nm FinFET technology, achieving significant improvements in energy efficiency and performance. The design delivers a low power-delay product, with a fast carry propagation delay (214.9 ps) and minimal power consumption, even at varying power-clock frequencies. The hybrid approach strikes an effective balance between compactness, switching efficiency, and energy recovery, making it ideal for low-power arithmetic circuits in VLSI systems.

For future work, the proposed design can be extended to more complex circuits like multipliers or processors, further optimizing the power and delay trade-offs. Additionally, exploring the impact of further scaling down the technology node to 7nm and below, coupled with advanced energy recovery techniques, could lead to even greater performance enhancements.

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