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DESIGN AND ANALYSIS OF LATCH SENSE AMPLIFIER USED IN SRAM IC BY USING LOW POWER TECHNIQUES

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ABSTRACT
In todays advanced technological world, semiconductor chips are widely used in modern electronics devices, where low power consumption and compact size are essential. Static Random Access Memory (SRAM) plays an important role in meeting these requirements for efficient data storage. This study presents the design of a high-performance latch sense amplifier for SRAM application using low-power techniques, implemented with Cadence Virtuoso software. Different power reduction methods are explored to achieve an optimized design. The performance of the proposed sense amplifier is analyzed by adjusting key parameters such as transistor width-to-length ratio, supply voltage, and nano scale technology. The study also evaluates power consumption, response time and transistor count for various design approach to determine the most effective techniques. The proposed low-power sense amplifier demonstrate improved efficiency and performance.
Keywords: SRAM, High Speed, Cross-Coupled Sense Amplifier, Sense Amplifier; Low power, Decoder, Power, Delay, DRAM.

I. INTRODUCTION

High Speed memories, such as Static Random Access Memory (SRAM), play a vital role in modern digital systems by enabling fast and reliable data access. In SRAM, sense amplifiers are essential components that detects and amplify small differential signals from memory cells, allowing accurate interpretation of stored data. Since only one row of memory is accessed during a read operation, reach column typically requires a single sense amplifier, which helps in reducing circuit complexity and delay.

Designing high- speed and low power sense amplifier has become increasingly challenging due to the continuous scalling of memory cell size and advancement in complementary
Metal- oxide - semiconductors (CMOS) technology. As technology scales down, chip density increases, which can lead to higher power consumption and design complexity. Therefore, achieving low power consumption while maintaining high performance in CMOS- based SRAM designs is of significant importance. Scaling also helps integrate more components on a single chip, reducing parasitic effects and improving overall speed.

The sense amplifier performs two key functions:
Sensing and amplification of data signals. However its performance is highly dependent on supply voltage and circuit parameters. A reduction in supply voltage may degrade sensing accuracy and increase delay. Additionaly, the presence of multiple bitlines in memory arrays further contributes to sensing delay. To address these challenges, it is necessary to develop optimized sense amplifier designs that minimize delay while reducing power consumption.

This paper analyzes conventional sense amplifier designs along with their limitations and processes

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an improved high- performance design for SRAM application. The proposed approach focuses on reducing sensing delay and power consumption through the application of effective low- power techniques. In particular, the negative wordline techniques is utilized to enhance power efficiency and overall performance.

The Main contributions of this work are as follow:

1 Development of a high – performance sense amplifier circuits suitable for low – power SRAM integrated circuits (ICs).

2 Analysis of the impact of important parameters such as transistor Width –to- Length (W/L)ratio, supply voltage, and different nanometer technologies on power consumption and response time of the proposed design.

3 Comparative study of the proposed sense amplifier with exiting designs, including differential voltage sense amplifiers, cross- coupled sense amplifier, and latch- type sense amplifiers, based on performance.

1. Implementation and Design of SRAM cell

SRAM cell Design with Read and Write Sense Amplifier

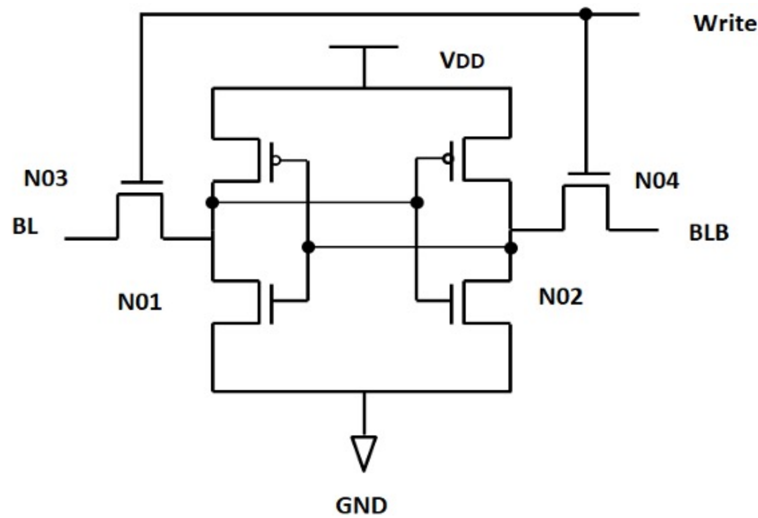

Figure 1. Static Random Access Memory (SRAM) Cell.

The Sense amplifier plays an important role in both read and write operation of SRAM cell by detecting and amplifying small voltage difference on the bitlines.

2.1 Read operation:

During the read operation, both bitlines (BL and BLB) are first precharge to a high voltage (VDD). When the word line (Write) is activated, the SRAM cell connects to the bit lines. Depending on the stored data (0 or 1), a small voltage difference is created between BL and BLB. The sense amplifier detects this small difference and quickly amplifies it to a full logic level (either 0 or VDD). This allows accurate and fast data reading.

Write Operation:

In the write operation, data is written into the SRAM cell through the bit lines. One bit line is set to high voltage (VDD) and the other to low voltage (ground), depending on the data to be written . When the word line (Write) is enabled, this voltage difference forces the internal amplifier assists in stabilizing the new value, ensuring reliable data storage.
Overall, the sense amplifier improves the speed, accuracy, and efficiency of both read and write operation in SRAM circuits.

2.2 Precharge

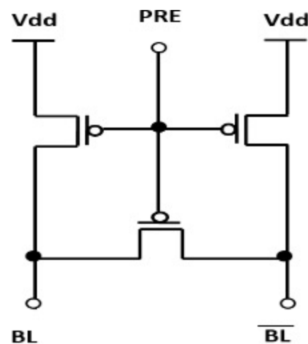

Figure 2. Precharge Circuit for Sense Amplifier

SRAM Architecture With Sense Amplifier:

The Differential sense amplifier is a widely used circuit in modern memory systems due to its high sensitivity and fast operation. It is primerly designed to detect and amplify small voltage difference between two input signals.
The circuit consists of a differential pair of NMOS transistors (N01 and N02). Whose gates are connected to the input voltage Vin1 and Vin2. These transistors are connected to the bit lines and act as the input stage of the amplifier. The output is typically taken from one side of the circuit, depending on the design requirements.
An active current mirror load, formed by PMOS transistors (P01 and P02), is connected at the top of the circuits. These PMOS transistors provide high gain and act as load elements improving the overall amplification capability of the circuits.
At the bottom of the circuits , a current source transistors is connected , which supplies a constant bias current to the differential pair, this current is shared between (N01 and N02) based on the difference between the input voltage . The use of a constant current source ensures stable operation and enhance the sensitivity of the amplifier.
The working principle of the circuit is based on current steering. When a small voltage difference exists between Vin1 and Vin2, the current through the differential pair is unequally distributed. This imbalance is converted into a voltage difference at the output node by the active load, resulting in amplification of the signal.
Since the total current supplied by the current source remains constant, any increase in current through one transistor results in a corresponding decrease in the other. This property enables precise detection of small input variations. The transient response of the differential sense amplifier is determined by the switching behavior of the transistors and the capacitive load present at the output.

Due to its high gain and fast response, the differential sense amplifier is highly suitable for sensing operations in SRAM and other memory circuits.

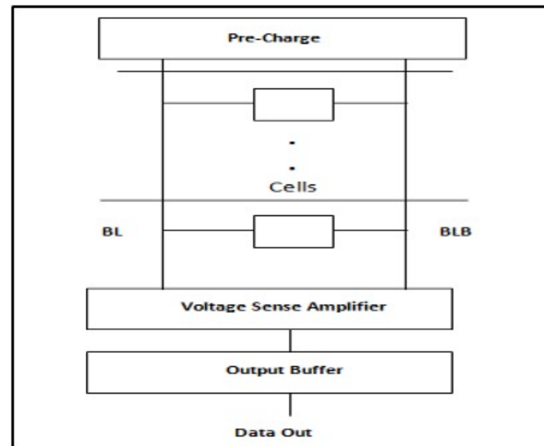

Figure 3. SRAM Model with Sense Amplifier.

2.3 Figure 3 shows the basic structure of an SRAM system integrated with a sense amplifier. The main components include the pre- charge circuit, memory cells, bit lines (BL and BLB), sense amplifier , output buffer, and data output stage.

2.4 At the begning of operation , the pre- charge circuit charges both bit lines (BL and BLB) to a high voltage level(VDD). This ensure that the system starts from a stable and equal condition before reading data.

2.5 The SRAM cells are connected between the bit lines. When a word line is activated, a selected memory cell interacts with the bit lines and creates a small voltage difference based on the stored data (0 or 1). The sense amplifier detects this small voltage difference between BL and BLB and amplifies it to a full logic level. This amplification is very fast and improves the accuracy of the read operation.

Word lines and Sense Amplifier Operation

Each memory cell is connected to a line called a word line, which is activated by applying a specific voltage. The voltage level for each word line is determined by the technology node used in the transistor design. This article focuses on the sense amplifier implementation at the 180 nm technology node, where the voltage level is set at

1.8 V. Each sense amplifier is connected to two complementary lines, interacting with both the word line and the bit lines. The same bit lines are used for both reading and writing data.

2.6 SRAM Operation: In read mode, the word line is set to high, activating the cell in that row. The stored values, 0 and 1, create a differential signal that the sense amplifier, located at the end of the lines, amplifies to a normal logic level. The bit from the requested cell is then latched into a buffer and sent to the output bus.

2.7 Sense Amplifier Goals and Types

The primary goals of a sense amplifier are to reduce sensing delay, increase amplification, minimize power consumption, fit within the allotted space, and ensure high reliability.

2.8 Types of Sense Amplifiers

A. Differential Sense Amplifier Design:

The Differential sense amplifier is a widely used circuit in modern memory systems due to its high sensitivity and fast operation. It is primerly designed to detect and amplify small voltage difference between two input signals.

The circuit consists of a differential pair of NMOS transistors (N1 and N2). Whose gates are connected to the input voltage Vin1 and Vin2. These transistors are connected to the bit lines and act as the input stage of the amplifier. The output is typically taken from one side of the circuit, depending on the design requirements.

An active current mirror load, formed by PMOS transistors (P1 and P2), is connected at the top of the circuits. These PMOS transistors provide high gain and act as load elements , improving the overall amplification capability of the circuits.

At the bottom of the circuits , a current source transistors is connected , which supplies a constant bias current to the differential pair, this current is shared between (N1 and N2)based on the difference between the input voltage . The use of a constant current source ensures stable operation and enhance the sensitivity of the amplifier.

The working principle of the circuit is based on current steering. When a small voltage difference exists between Vin1 and Vin2, the current through the differential pair is unequally distributed. This imbalance is converted into a voltage difference at the output node by the active load, resulting in amplification of the signal.

Since the total current supplied by the current source remains constant, any increase in current through one transistor results in a corresponding decrease in the other. This property enables precise detection of small input variations. The transient response of the differential sense amplifier is determined by the switching behavior of the transistors and the capacitive load present at the output. Due to its high gain and fast response, the differential sense amplifier is highly suitable for sensing operations in SRAM and other memory circuits.

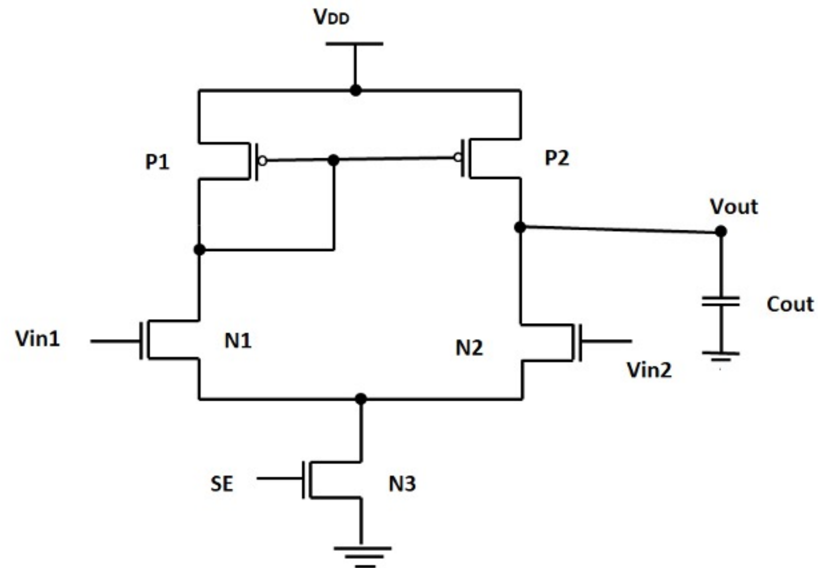

Figure 4. Differential Sense Amplifier Schematics

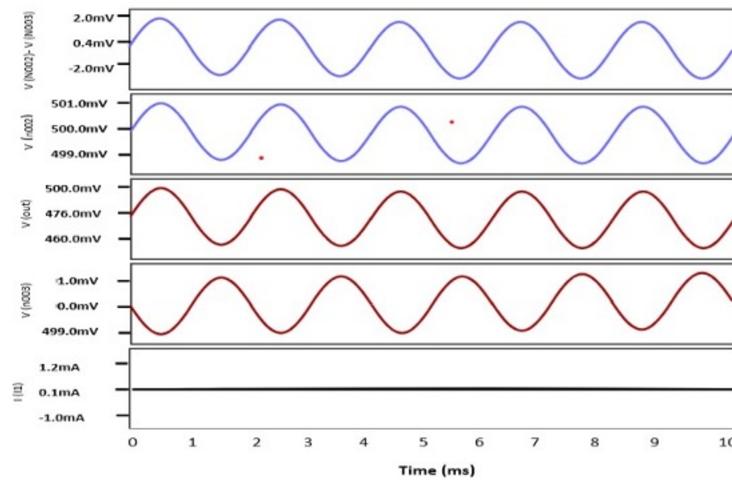

Figure 5. Output waveform of Differential Voltage Sense Amplifier.

B. Basic Latch- Based Sense Amplifier

a. The basic latched sense amplifier us a static voltage- mode sensing circuits widely employed in high- speed memory architecture such as SRAM. It is designed to detect very small voltage differences on bit lines and rapidly amplify them into full logic levels using regenerative positive feedback. Due to its high sensitivity and fast decision- maiking capability, it plays a critical role in read operations of memory systems.

b. The basic latched sense amplifier consists of two cross- coupled CMOS inverters formed by transistors (P1-P2) and (N1-N2). These inverters are interconnected is a feedback configuration such that the output of one inverters is fed to the input of the other, forming a bistable latch. The inputs to the sense amplifier are provided through complementary bit lines, namely BL and BLB. These bit

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lines carry a small differential voltage generated during the memory read operation. A PMOS transistors (P3) is connected between the supply voltage (VDD) and the latch structure. It is controlled by the signal SEB (Sense Enable Bar) and is responsible for precharging and initializing the internal nodes of the circuit. At the bottom, an NMOS transistor (N3) is connected to ground and controlled by the Sense Enable (SE) signal. This transistors acts as a tail switch, enabling the sensing operation when activated.

c. During the precharge phase , both bit lines (BL and BLB)are charged to an equal voltage level, typically close to VDD. This ensures a balanced initial condition for accurate sensing.

d. When a memory cell is accessed, a small voltage difference develops between BL and BLB depending on the stored data. However, this voltage difference is typically very small and cannot be directly interpreted as a logic levels.

e. The basic latched sense amplifier provides an efficient solution for fast and accurate sensing of small differential signals in memory circuits. Its regenerative feedback mechanism ensures rapid amplification and stable latching. Making it a fundamental components in modern high- performance memory designs.

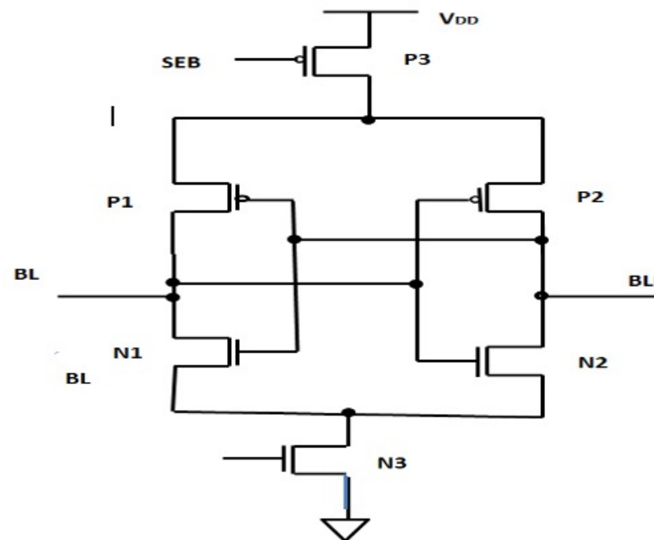

Figure 6. Basic Latched Sense Amplifier Schematic.

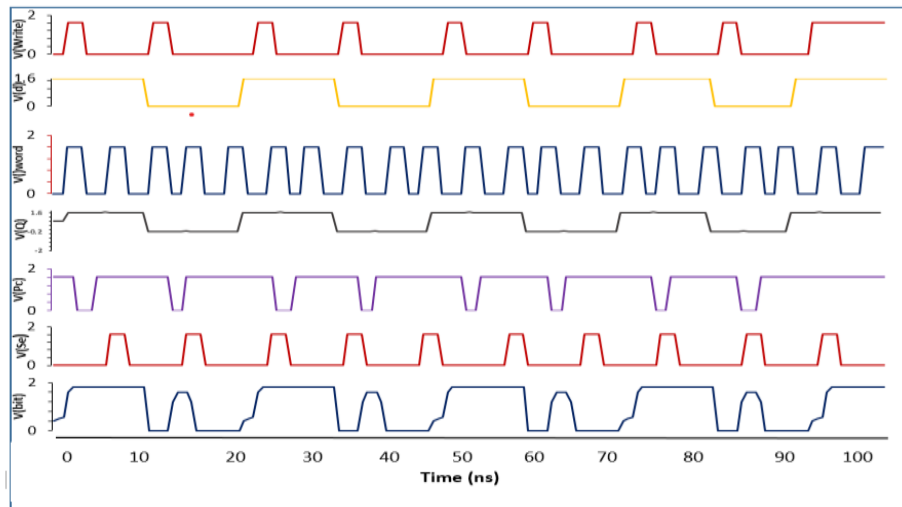

Figure 7. Output waveform of Basic Latch Sense Amplifier.

C. Block Model of Basic Latched Sense Amplifier Architecture (Modified)

The modified basic latched sense amplifier is an enhance version of the conventional latch- type sense amplifier, designed to improve sensing accuracy and control bit- line behavior during operation. The core of the circuit consists of two cross- coupled CMOS transistors formed by (P1-N1) and (P2-N2). These transistors are connected in a regenerative feedback configuration, which enables fast amplification and latching of small voltage differences. In this modified design, additional transistors (P3 and P4) are inserted between the bit lines (BL and BLB) and the internal nodes of the latch. These transistors act as access or isolation devices, controlling the connection between the bit lines and the sense amplifier. A PMOS transistors (P5) is connected to the supply voltage (VDD) and is controlled by the signal SEB (Sense Enable Bar). It is responsible for precharging and initializing the internal nodes of the circuit. At the bottom, an NMOS (N3) is connected to ground and controlled by the sense enable (SE) signal. It acts as a tail transistor that that enables current flow during the sensing phase.

During the precharge phase, both bit lines (BL and BLB) are charged to the same voltage level ,ensuring a balanced initial condition. When a memory cell is accessed, a small voltage difference develops between BL and BLB depending on the stored data. This difference is initially very small. Before the sense amplifier is fully activated, the access transistors (P3 and P4) allow the internal nodes of the latch to track the bit- line voltage. At the same time, they control the discharge of the bit lines, preventing excessive power loss.

The NMOS transistor (N3) turns ON, activating the latch.

The PMOS transistors (P5) provides proper biasing.

The access transistors (P3 and P4) starts isolating the bit lines from the internal nodes.

Due to the cross- coupled inverter configuration, regenerative positive feedback is established. Even a small

Voltage difference between the internal nodes is rapidly amplified.

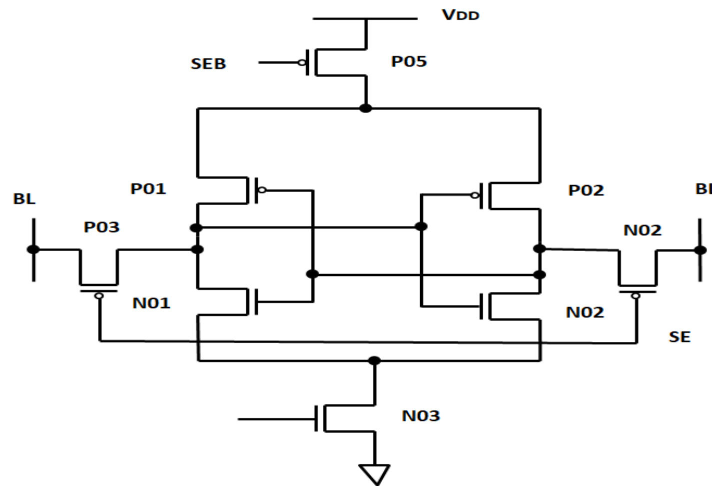

Figure 8. Basic Latched Sense Amplifier (Modified)

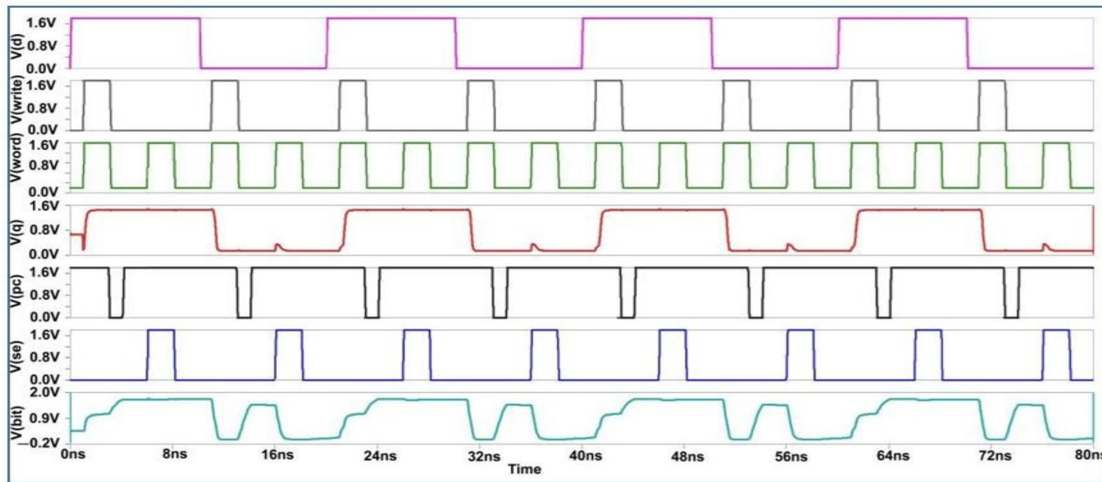

Figure 9. Output waveform of Basic Latch Sense Amplifier (Modified)

Exploring the Impact of Power Reduction Techniques on Conventional Sense Amplifier Design

A Power Reduction Methods

This section presents different circuit-level techniques used to reduce leakage power in a 6T SRAM cell. These methods mainly work by controlling the terminal voltages of the SRAM cell during standby mode, thereby minimizing unnecessary power loss.

1 Sleep Transistor Technique

In this technique, a PMOS transistor is connected between VDD and the SRAM cell, while an NMOS transistor is placed between the SRAM cell and GND. Both transistors are activated in the active mode, establishing a pathway between VDD and GND. During active mode, both transistors are turned ON, allowing a direct path between VDD and GND, so the circuit operates normally.

In sleep mode, both transistors are turned OFF, which disconnects the power supply from the SRAM cell. This creates a virtual VDD and GND, effectively reducing leakage power.

Source Biasing Technique

In this techniques, a negative voltage is applied to the word line during idle (standby) condition. This increases the threshold voltage of transistors, which helps in reducing leakage current.
When NMOS transistors are negatively biased and PMOS are positively biased, the leakage current is significantly minimized. Studies show that applying around-0.4V can effectively reduce leakage power.

Dual Sleep Technique

This techniques uses two pairs of transistors(PMOS and NMOS) connected in parallel.
One pair is placed between VDD and the SRAM cell.
The other pair is placed between the SRAM cell and GND.
During active mode, both pairs are ON, allowing normal circuit operation.
During sleep mode, both pairs are turned OFF, disconnecting the power supply and ground. This creates virtual VDD and GND, which reduces leakage power more effectively compared to single sleep transistor techniques.

Table1.Comparison of average power consumption with varying supply voltage for various sense amplifiers P (µW) for180nm

S.N.	**Basic Latch Sense Amplifier[7]**	**Basic Latch Sense Amplifier with Pass Transistor [5]Modified**
1	36.425	36.627
2	55.412	55.656
3	80.990	81.061
4	96.995	90.227
5	108.770	114.40

Block Model of Modified Standard Sense Amplifier:

The modified latch sense amplifier is designed to efficiently detects and amplify small voltage differences between the bit lines(BL and BLB) of an SRAM cell. The circuit mainly consists of cross- coupled PMOS(P1,P2,P3) and NMOS (N1,N2,N3,N4) transistors, forming a regenerative latch structures.

Pre Charge Phase:

During the pre- charge phase, both bit lines(BL and BLB) are charged to a high voltage level (approximately equal to VDD).

The sense amplifier remains inactive in this phase.

The control signal SEB (Sense Enable Bar) keeps the circuit disabled.
No current flows through the latch, ensuring low power consumption.

Evaluation Phase:

When the word line of the SRAM cell is activated, a small voltage difference is developed between BL and BLB depending on the stored data.
This small voltage difference is the input to the sense amplifier.

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Sense Amplification(Latch Operation):

When the SEB signal goes LOW, the sense amplifier is enabled.
Transistor P3 and N1/N2 active the latch structure.
Cross- coupled transistors (P1-P2 and N3-N4) provide positive feedback.
Even a very small voltage difference between BL and BLB is quickly amplified.

For Example:
If BL>BLB- P1 turns OFF slightly, P2 turns ON strongly.
This pulls BLB further down and BL up, reinforcing the difference. This regenerative action rapidly
Converts the small input difference into full logic levels.

Output Stabilization:
One node goes to VDD (logic1)
The other node goes to GND (logic0)
Thus, the sense amplifier produces a clear and stable digital output.

Key Advantages of Modified Design:
Faster sensing due to strong positive feedback
Reduce power consumption using controlled enable signal (SEB)
Improved Sensitivity to small voltage differences
Better performance compared to conventional latch sense amplifiers

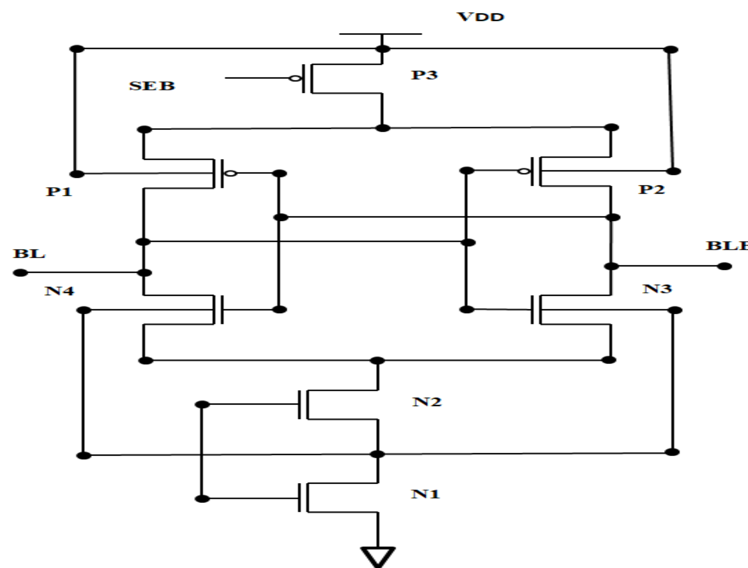

Figure 10. Schematic of Modified Latch Sense Amplifier

The modified latch sense amplifier improves sensing speed and reduces power consumption by using an efficient latch structure and controlled activation through the SEB signal. The regenerative feedback mechanism ensures accurate and fast amplification of small bit- lines voltage differences, making it suitable for low-power SRAM applications.

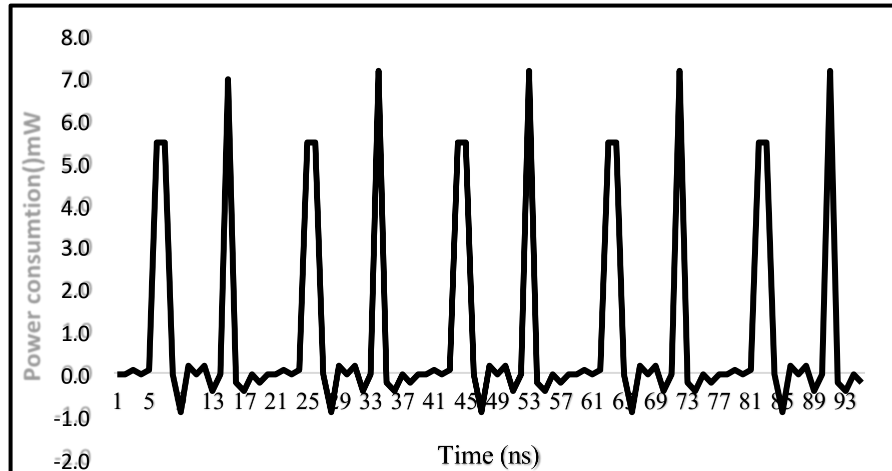

Figure11.Power Consumption Spectrum of Modified Basic Latch Sense Amplifier.

The average power consumption of the modified sense amplifier is analyzed using 180nm CMOS technology. The results demonstrate that power consumption increases with the rise in supply voltage (VDD), which is a common trend observed in all sense amplifier architectures.
The power consumption waveform (figure) shows distinct transient peaks during the evaluation phase, representing dynamic switching activity. These peaks occur due to charging and discharging of internal nodes during the sensing operation.
The proposed design enhances sensing performances by rapidly amplifying small voltage differences between bit lines while reducing static and dynamic power losses. As a result, the sense amplifier achieves an optimal balance between speed and power, with an average power consumption of approximately7.2mW.

S.N.	Design Name	Supply Voltage	N0. of Transistor used
1	Differential sense amplifier [8]	1.8	4
2	Basic Latched Sense Amplifier[7]	1.8	6
3	Basic Latch sense Amplifier with pass transistor[5] Modified	1.8	8

II. PROPOSED SENSE AMPLIFIER: IMPLEMENTATION, RESULTS AND DISCUSSION

The proposed design is modified cross-coupled sense amplifier, which is used to detect small voltage difference between the nit lines (BL and BLB) and converts them into a full digital output.

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In this circuit, transistors P1,N1 and N2 from the main sensing path, while N3 and N4 act as access transistors controlled by the write signal. The SE (Sense Enable) signal controls the activation of the sensing operation.

During operation , when the write signal is active, the bit line (BLB) is connected to the circuit through transistors N3nad N4. A small voltage difference is developed at the output nodes (Out and OutB).

When the SE signal is enabled, transistors N1 turns ON, allowing current to flow towords ground. This activates the cross- coupled structure, and due to positive feedback, the small voltage difference between the nodes is quickly amplified.

As a Result:

One output node (Out) goes to HIGH(VDD)

The other node (OutB) goes to LOW (GND)

This shows that the circuit successfully converts that the proposed design operates with stable switching behavior and controlled power consumption. The power spikes occur only during switching , which indicates efficient dynamic operation.

Compared to basic sense amplifiers, the proposed design provides:

Faster sensing speed.

Reduce power consumption .

Better stability during operation.

Additionally, the use of control signals like write and SE helps in reducing unnecessary power usage by actively the circuit only when required. The design also performs well at low voltage, where traditional sense amplifiers face difficulty. This makes the proposed circuit suitable for low- power and high-speed SRAM applications.

Overall, the proposed modified cross- coupled sense amplifier improves performance by providing fast, stable, and power- efficient operation.

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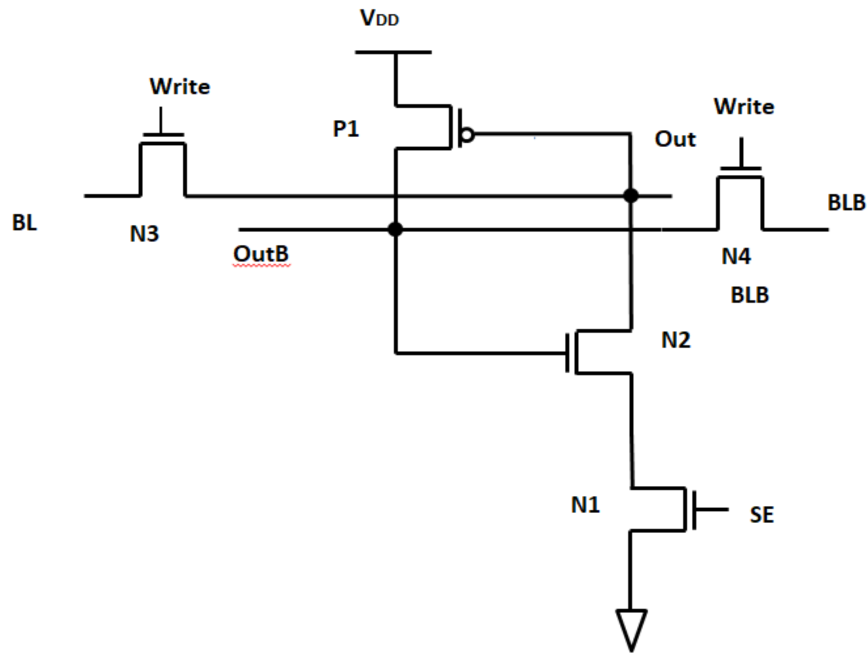

Figure12.Schematic of Proposed design (Modified Cross-Coupled SRAM).

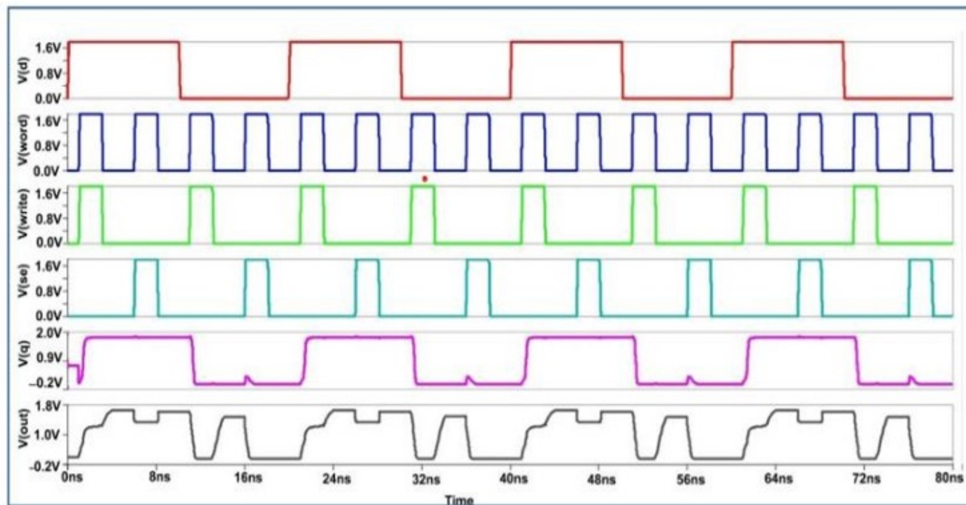

Figure13.Output Waveform of Proposed Sense Amplifier.

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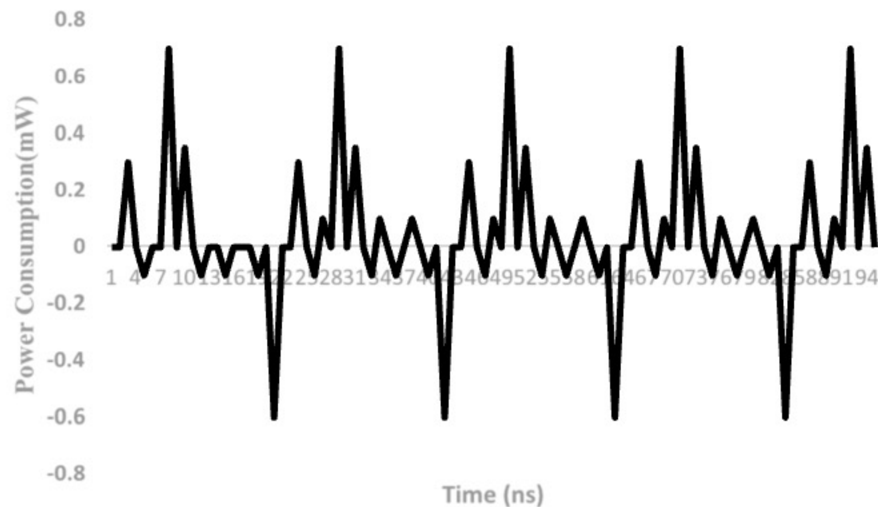

Figure14. Power Consumption wave of Proposed Sense Amplifier.

The results indicates that techniques aimed at reducing power consumption also contribute to lowering access time in large memory systems. By integration a cross – coupled FET configuration with negative word line and source biasing techniques, the proposed design effectively minimizes bit – line capacitance, thereby reducing RC delay. This Improvement is consistent with the modified cross- coupled design illustrated in figure.

In the proposed design, during the READ operation , a negative bit- line technique is incorporated, which performs a function similar to source biasing by applying a negative voltage to the word line during idle conditions. This approach does not degrades device performance or significantly impact the soft error rate. Additionaly, it reduces sub- threshold leakage current by turning off the access transistors.

However, a potential limitation of this method is the increase in gate leakage current due to larger gate-to-source and gate-to drain voltage differences. Despite this drawback, the technique helps stabilize the write signal within a narrow range, ultimately resulting in a noticeable reduction in overall power consumption.

Figure is present the static noise margin (SNM) analysis for hold, read and write operations of the proposed sense amplifier in SRAM. The results demonstrate strong noise immunity, which is essential for reliable memory operation. A higher SNM indicate improved signal stability and robustness during read and write processes.
Compared to circuits with longer operation delays, the proposed design achieves faster operation, making it suitable for high- speed SRAM applications. During the write operation, when both the word line and signal are set to High (logic 1), data is transferred from node D to node Q. In the read operation, the circuit is first precharged , and the logic 1 to one side of the SRAM cell, the bit line does not fully charge to VDD due to the threshold voltage drop across the NMOS transistors,

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resulting in a slight voltage drop at the output node. Meanwhile , the complementary bit line is fully discharged.

This voltage difference is sufficient to trigger the cell onto the desired state. The precharge signal is then set to logic 0 , allowing the PMOS transistor to fully charge the bit lines to VDD. During the read operation, both the word line and SE signal must be activated simultaneously to transfer the stored data from the internal node to the output.

S.N.	**Design Name**	**Area (Transistors)**	**Power Consumed (µW)**	**Area (Transistors)**	**Power Consumed (µW)**
1	**Basic Latch Sense Amplifier [7]**	**6**	80.723	**6**	**39.5040**
2	**Basic Latched Sense Amplifier with Pass Transistor[5] Modified**	**8**	81.0602	**8**	**9.460**
3	**Proposed Design**	**5**	80.65	**5**	**6.9900**

Table2.Comparison of average power consumption for all the designs with their modified versions.
Table 3 presents a comparative analysis of different sense amplifier design in terms of transistor count and average power consumption. The comparison includes both conventional and modified configuration to highlight the effectiveness of power reduction techniques.
It can be observed that the basic latch sense amplifier consumes relatively higher power in both its original and modified forms. The basic latched sense amplifier with pass transistors shows a slight improvement in power efficiency after modification.

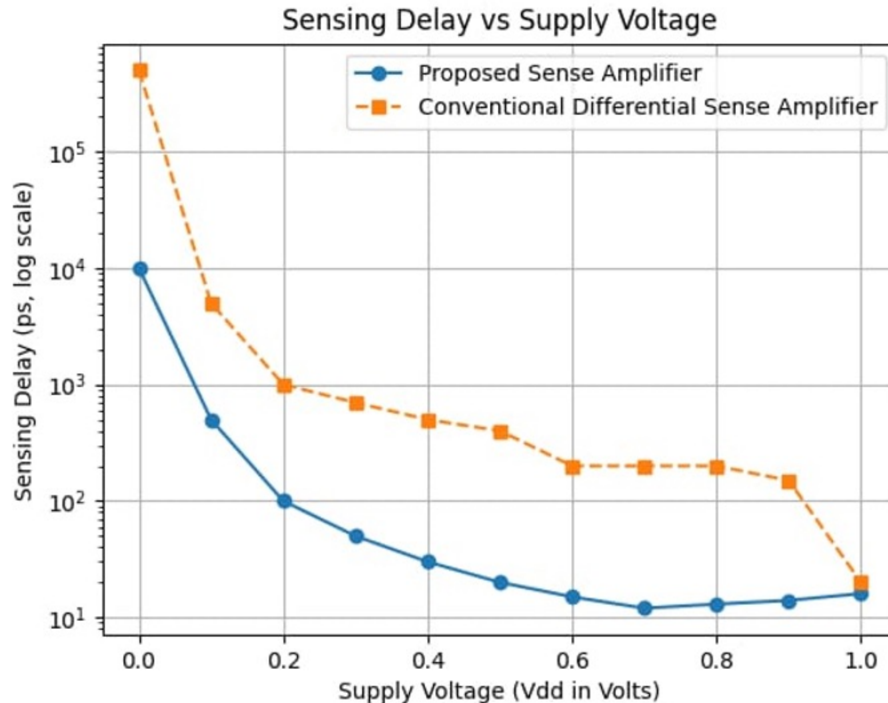

Figure 15. Sensing Delay of Proposed Sense Amplifier.

Figure 15 illustrates the sensing delay performance of the proposed sense amplifier as a function of supply voltage. The overall performance of the sense amplifier is primarily determined by its sensing delay.

By incorporating negative bit line and modified cross- coupled SRAM design achieves a significant reduction in sensing delay compared to the conventional differential sense amplifier. At a low power supply voltage of 0.1V, the proposed design demonstrate a substantial reduction in delay, nearly 99%, due to the minimized capacitance effect on the bit lines, which effectively reduces latency. This reduction in capacitance is achieved by applying a negative voltage to the word line, while maintaining stability in terms of noise margin, power consumption, ans delay performance. Furthermore as the supply voltage increases from 0.1V to 1.0V, the sensing delay consistently decreases from approximately 5.5ns to 55ps, indicating improved speed and efficiency of the proposed design.

Future Scope :

The Proposed modified cross-coupled sense amplifier can be further improved using advanced CMOS technologies such as 45nm and Fin FET technology for achieving lower power consumption and higher operating speed. In furure work, the circuit may be optimized for ultra - low voltage applications to enhance battery efficiency in portable and IoT devices. The proposed design can be integrated into high-speed SRAM cache memories, AI processors, embedded systems, and edge

computing applications. Future research may focus on improving stability, reducing noise sensitivity, and minimizing process variation effects for reliablr operation in modern VLSI systems.

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